# OR1K programming notes

WARNING: names of the registers and their ID numbers will change in the future. And yes, we are working on real documentation, please be patient.

**GPRs**

OR1K has only 15 GPRs (r0 is hardwired to zero). They are r1-r15. This is due to a fact that OR1K implementations will be used in FPGAs and ASICs in embedded and similar environments. r1 is stack pointer, r2 is frame pointer (if required). Link register was until recently r11 but this is about to change (see special reg LR).

Flags (a.k.a. CR or CCR) are not directly accessible. It is possible this will change and they will be accessible as one of the special regs.

**Exceptions**

Current PC is saved to EPC. If I-TLB, D-TLB miss or one of page fault exceptions EEA is set with effective address in question. Other registers must be saved by exception handler routine. Processing continues from:

0x100: reset
0x200: machine check exception (bus error and similar)
0x300: data page fault exception
0x400: insn page fault exception
0x500: external interrupt
0x600: alignment exception
0x700: illegal insn exception
0xC00: syscall
0x1300: breakpoint exception

Probably some additional exceptions will be added. And the numbers will change (I copied them from PPC since I just couldn't remember my own).

**Coprocessors and Special registers**

Registers of coprocessors are grouped into 16 groups (16 coprocessor domains). Each group can have 4096 registers. A coprocessor can occupy two or more group register spaces. Instructions to read and write registers are mtsr and mfsr.

Group access

| Register Range | Access in User Mode | Access in Supervisor Mode |
|---|---|---|
| 0-1023 | R/W | R/W |
| 1024-2047 | Read only | R/W |
| 2048-3071 | Inaccessible | R/W |
| 3072-4095 | Inaccessible | Read only |

Official groups

| Group Number | Coprocessor Function |
|---|---|
| 0 | System registers |
| 1 | Data MMU (or in case of joint data and instruction MMU) |
| 2 | Instruction MMU |
| 3 | Data Cache |

| | |
|---|---|
| 4 | Instruction Cache |
| 5 | Performance Monitor Unit |
| 6 | Debug Unit |
| 7 | Time Base Unit |
| 8-11 | Reserved for future use |
| 12-15 | Custom coprocessors |

Group 0

| Register Number | Register Name | Description |
|---|---|---|
| | | |
| 1 | CTR | Counter register |
| 2 | LR | Link register |
| | | |
| 2048 | EPC | Exception PC |
| 3072 | MSR | Machine Status Register (user/supervisor mode, trace, exceptions enabled/disabled etc.) |
| 3073 | CPCFG | Coprocessors Configuration |
| 3074 | EEA | Exception EA |
| | | |
| | | |

MSR:

| 31 - 4 | 1 | 0 |
|---|---|---|
| Reserved | Interrupt Enable | User (0) / Supervisor (1) |