If the full 56K memory capability is not desired, it is possible t
code to allow the MP-09 processor board to run in an unmodified 680

Alter Direct Page Register - control "D"

The alter direct page register command takes the following format:

```
>^D     DP=00 01                                    -alter direct page register to $01
```

Alter Program Counter - control "P"

The alter program counter command has the following format:

```
>^P     PC=4655 434B
```

Examine Memory - "E [addr] -[addr] "

Display Registers - "R"

The display register command causes the SBUG-E© monitor to display the contents of all accessible processor registers. Most register values are displayed in hexadecimal, however, the condition code register is shown in an expanded binary format. If a flag bit in the condition code register is set the corresponding flag name is shown, otherwise the flag position is denoted with a hyphen. The format of the display is as follows:

```
- SP=hhhh US=hhhh DP=hh IX=hhhh IY=hhhh
- PC=hhhh A=hh B=hh CC: E F H I N Z V C
```

Fast Maskable Interrupt Vector - $DFC6

This vector contains the address of the FIRQ interrupt service routine. After power up processing, this vector points at a return from interrupt instruction.

Software Interrupt II Vector -$DFC4

This vector contains the address of the secondary software interrupt service routine entered whenever an SWI2 instruction is executed. After power up, this vector points to a return from interrupt instruction. The secondary software interrupt is not used on a system level to make it available at a user level.

Software Interrupt III Vector - $DFC2

This vector contains the address of the tertiary software interrupt service routine entered whean S