CPUGEN TUTORIAL V1.00

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Getting start

- 1) Decompress cpugen.zip inside a working directory (ex. C:\cpugen)
- 2) Add the working directory into the windows PATH

Cpu4Bit

Goal:

- compare 4 digital input with 4 fixed thresolds and move a PWM output consequently

CPU 4 bit => Data Bus Length Word = 4

If I use a 8 bit Istruction Words Length (the minimum length), I have a 16 word (8-4) istruction page size (too small), so I need a 10 bit Istruction Words Length => 64 word istruction page size. The source code (Asm) isn't too long so 256 rom words (8) are enough. Istruction Address bus = 8 = 4 pages of 64 words each.

I have 16 nibble of RAM, a control register and a PWM peripheral.

Altera Design:
Start cpu4bit.quartus in cpu4bit\Altera directory.
EAB (Embedded Array Blocks) are used for ram (ram.mif) and rom (rom.mif). In Assignments\Device I choice the ACEX1K device and Auto Selected.

Cpu8Bit

cpugen

Goal:

Run - -

CPU 8 bit => Data Bus Length Word = 8 I use a 14 bit Istruction Words Length, so I have a 10 bit (14-4) istruction/data addressing capability => 1K words of

I need interrupt and indirect addressing support.
I set a 8 deep stack (see Help/CpuCore: How to set stack deep)

Code structure:

1)

1) Simulate it with Quartus Waveform simulator:

Cpu16Bit

EAF Rem 1(evi).7(mce)6 RgH d	3 (Embedded Array I neo)3.9(e)- nra tœ c8.(h).6.4oi).7(mce)t	Blocks) are used for ra rand d Upd a8.53(t)(c mh-5147(e C)996(Y-5	m (ram.mif) and rom b)-heea-oc-n-514(chn 5141(C).76(L7.4(iON	(rom.mif). id).6(g).6()8smwcpu).69(E dev).6.4i).7(m	1 ce)EP6.46(1C)996(3T7.4	4(i1).6.400C)996(

Altera Design:

Start cpu16bit.quartus in cpu16bit\Altera directory.

Design flow

Steps for a new design:

- 1) Define what processor have to do
- 2) Decide a first cpu architecture
- 3) Set the cpu parameters
- 4)

Bibliography: