```
        -- assign combined DAT_O signals
        DAT_Oa <= SDAT_Oa when (CYC_Oa = '1') else MDAT_Oa;
        DAT_Ob <= SDAT_Ob when (CYC_Ob = '1') else MDAT_Ob;
end architecture dataflow;
```

The figure below shows some timing diagrams displaying the MASTER/SLAVE selection of the cores. Note that when both MASTER interfaces assert ('1') their [CYC_O] signal at the same time, coreB is selected as the SLAVE interface ([CYC_Ob] is asserted), i.e. coreA has the highest priority. The SLAVE interface remains selected until the MASTER interface negates ('0') its [CYC_O] signal.

2.3 Bus Cycle signals

By inserting tri-state buffers almost all bus cycle signals can be combined. But this is